A Power Gating Scheme for Ground Bounce Reduction during Mode Transition

Ku He
Dept. of Electronic Engineering, Tsinghua University, Beijing, 100084, China
heku00@mails.tsinghua.edu.cn

Rong Luo
Dept. of Electronic Engineering, Tsinghua University, Beijing, 100084, China
luorong@tsinghua.edu.cn

Yu Wang
Dept. of Electronic Engineering, Tsinghua University, Beijing, 100084, China

Abstract

Power gating is an effective method to reduce leakage power during the circuit sleep mode; however, it introduces the ground bounce problem and has considerable energy consumption during the mode transitions. To mitigate the ground bounce, we propose a novel power gating scheme that reduces the magnitude of the peak current and voltage glitches as well as the time to stabilize power and ground during mode transitions. To further decrease the wakeup time while keep the energy efficiency, we introduce two improved circuit schemes with two intermediate states, based on our proposed power gating scheme. The scheme provides an average peak voltage reduction of 67.0%, and the wakeup time reduction is up to 62.3%. If the circuits use the intermediate schemes, wakeup time can be further reduced by a maximum of 95.7%. Beside these reductions, our proposed circuit scheme also has the advantage of small size and flexible controllability.

1. Introduction

The shrinking of operating voltage and device sizes reduce dynamic power for low power integrated circuit designs; however, it introduces other problems, such as larger leakage power and lower noise margin. To mitigate the leakage problem, power gating and Multi-Threshold CMOS (MTCMOS) are widely implemented [1] to suppress the leakage power in standby mode. Sleep transistors (ST), which are used to gate the power, deteriorate the noise characteristic of the circuits because their drain to source voltage drop changes the virtual rails of the circuit. Furthermore, during the mode transitions: especially from sleep mode to active mode, the power gating schemes cause large power and ground bounce that greatly affects the reliability of the circuits nearby in a mixed signal design. Another problem is the extra energy during the mode transitions in a power gating design.

Many methods have been proposed for ground bounce reduction and mode transition energy saving. Kim *et al*. [2] proposed a novel power gating structure, in which V_{GS} or the effective size of the ST increases dynamically in non-uniform stepwise manner to mitigate the ground bounce. This method can greatly reduce the ground bounce, but require complex control logic, and the ST must be carefully sized. Deogun *et al*.[3] also proposed a similar structure, and they introduced a continuously variable intermediate mode, which broadened the scope of soft gating. However, this method also required a complex control circuitry. Pakbaznia *et al*. [4] analyzed the charge recycling technique and its effect on ground bounce. The technique required two power gating structures with an NMOS and a PMOS ST separately, and can achieve up to a short-term maximum energy saving of 50% in applications with relatively small sleep periods.

The ground bounce not only depends on the discharge/charge current rate dI/dt of the circuit, but also depends on the gated circuits' inherent characteristics, i.e. the dump coefficients, the number of zero/pole points. Therefore, the effects of the ground bounce reduction techniques are quite difficult to compare concerning different process technologies. In this paper, we present an initial research on ground bounce reduction; the further research should be our future work, which requires better investigation on the modeling of transistors, pads and circuit boards.

In order to reduce ground bounce, we propose a novel power gating scheme, which utilizes the fact that a diode can be replaced by a transistor. Furthermore, the diode can be made controllable by adding an additional transistor, as shown in Figure 1. Our work has two major contributions to ground bounce reduction during mode transitions:

1-4244-1258-7/07/$25.00 ©2007 IEEE

1). During wakeup procedure, our power gating scheme, which implements a small transistor to control the ST, has two stages: relaxation stage and completely turn-on stage. During the relaxation stage, the V_{DS} of the ST reduces significantly while limiting the current exponentially as the $V_{DS,ST}$ changes. Our scheme has the advantage of using the ST itself to limit the discharge current, thus make the circuit quite simple. Also, it avoids using analog signals (like stepwise V_{GS} mentioned above) to control ST, and the control signal is relatively easier to generate. During the complete turn-on stage, the small control transistor is turned off, and the ST acts like a current source. This two-stage transition method reduces the peak voltage fluctuations in the virtual ground and virtual power, and it also reduces the circuit wakeup time.

2) We introduce two circuit schemes with intermediate states to further reduce the ground bounce based on our proposed power gating circuit scheme. Meanwhile, the intermediate state saves more charges by charge recycling [4] while allowing the virtual ground or virtual power floating between V_{DD} and ground. Because of a longer leak path and lower transition energy, our second circuit scheme II achieves a better tradeoff between the leakage reduction and the wakeup time.

The paper is organized as follows. In Section 2, our novel power gating scheme is described. The improved circuits with intermediate states are proposed in Section 3. The implementation and experimental results are presented in Section 4. In Section 5, we conclude this paper.

2. Novel power gating scheme

In this section, we propose a novel power gating scheme in which the mode of ST is changed during circuit mode transitions.

In the general circuits using sleep transistors, some logic has separate power and ground pads, while other logic may share the power and ground pads, as shown in Figure 2. A certain length of PCB(Printed Circuit Board) transmission line connects each pad with the real power or ground. If the PCB has poorly layout, the transmission lines will contribute large parasitic capacitors and inductances, which can deteriorate the ground bounce effect when the sleep transistors are switched on. The parasitic capacitors, inductances depend largely on what types of the pads are and how the PCB layout is, however, many empirical data shows that these parasitic parameters can be quite considerable.

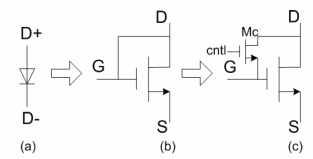


Figure 1. Diode and transistors

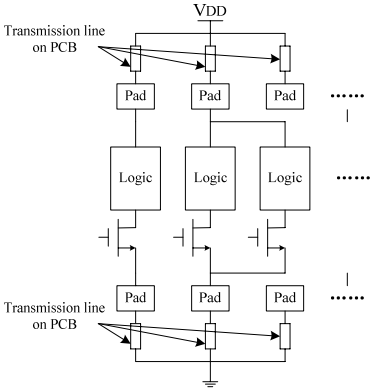


Figure 2. Logic using sleep transistors

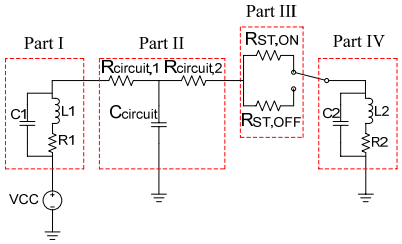


Figure 3. Equivalent circuits

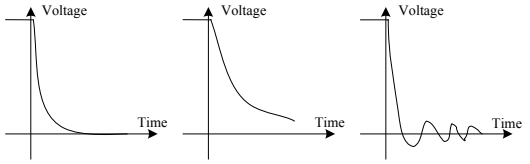


Figure 4. Impulse response curve of the sleep transistor circuits

The equivalent circuit of the logic using sleep transistors is shown in Figure 3. There are four parts of the equivalent circuit. Part I is the intrinsic capacitor, inductance and resistor of the power pad and the corresponding on-board transmission lines; Part II is the equivalent circuit of the functional logic; the sleep transistor is modeled as two resistors in Part III, where $R_{ST,\,ON} << R_{ST,\,OFF}$. When the sleep transistor is turned on, it equals a small resistor which has negligible effect on the normal function of the circuit. When the sleep transistor is turned off, its resistor becomes huge and cuts off the leakage path of the logic. Part IV is the intrinsic capacitor, inductance and resistor of the

ground pad and the corresponding on-board transmission lines.

The transmission function of the equivalent circuit has the form as follows:

$$H(s) = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (1)$$

The impulse response curve in time domain can have three forms according to the coefficients b_3~b_0, a_5~a_0, as shown in Figure 4 (a), (b), (c). (a) is the ideal situation since it requires minimum time for the slept logic to wake up, while (b) and (c) require much more time to wake up and may cause the ground bounce problems. Theoretically, the size of the sleep transistor and the circuit layout can be carefully designed to shape the response curve as Figure 4 (a), however, the process variation makes these designs impractical. From the response curves, we can also conclude that the sleep transistor sizing can affect the ground bounce. Small sleep transistors can provide large resistors, whose corresponding response curve is as Figure 4 (a), however, large resistor may cause large voltage drop over the sleep transistor, which may affect logical functionality.

Figure 5 shows the proposed scheme with an NMOS ST, whose size is determined using the method by Long [10]. During the active mode, the virtual ground and virtual power equal to 0 and V_{DD}, respectively. During the sleep mode, the ST is turned off to gate the power. If the sleep mode is long enough, the virtual ground will be charged up to a value near V_{DD}, while the virtual power will be discharged to a value near ground [6]. When the ST is fully turned on by a sharp 0→1 control signal, the virtual ground will be sharply discharged, causing a large transient current. This current further leads to a great fluctuation in the power-ground grid due to the parasite inductances and capacitances ($L_{1,2}$, $C_{1,2}$, $R_{1,2}$ shown in Figure 5) in the power and ground pins.

Assuming that sleep/wakeup or other control signals are supplied by an on-chip power management module, the essential idea to reduce the ground bounce during mode transition is to limit the large transient current. We notice that the virtual ground goes down sharply when the ST is turned on. If the edge of the virtual ground can be used as the control signal to limit the current, the ground bounce can be reduced. Diode (shown in Figure 1(a)) has such inherent characteristic for the current control, shown as the well-understood diode current equation (Eq.(2)):

$$I_D = I_S\left(e^{\frac{V_D}{V_t}} - 1\right) \quad (2)$$

In Eq.(1), as VD decreases, the current over the diode I_D decreases exponentially. However, we can not simply replace the ST with a diode, because a diode is not controllable. On the other hand, in practical circuit design, a transistor with drain and source connected is used as a diode, which is shown in Figure 1(b). This scheme is very close to the ST, and if a small transistor is inserted, as the M_C shown in Figure 1(c), we can obtain our proposed circuit scheme. This scheme provides a controllable path between the gate and drain of the ST. The turn-off and turn-on of the control transistor M_C make the ST work in the normal operation and the relaxation operation (working as a diode) respectively.

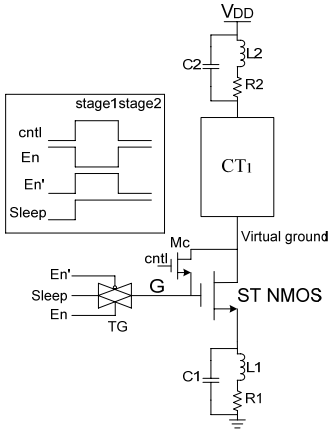


Figure 5. Proposed scheme for ground bound reduction

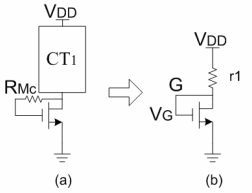


Figure 6. Equivalent circuit in relaxation stage

During the normal operation, the small transistor is turned off and has no impact on the ST. When the circuit is switched from sleep mode to active mode, which is more critical for the two kinds of mode transitions, there exits a two-stage procedure.

In stage I–the relaxation stage, the transmission gate TG is turned off and the sleep control signal is cut off, thus the node *G* is a floating node. And at the same time, the control transistor M_C is turned on to make ST working as a diode. The stored charge in the circuit CT_1 is discharged through the ST. The drain current of the ST during the relaxation stage is as Eq.(3). And the equivalent circuit is shown Figure 6.

$$I_d = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (3)$$

Since the drain-to-source voltage of the small transistor is 0, which makes $V_{DS} = V_{GS}$, the current I_d goes through the ST can be further interpreted as Eq. (4):

$$I_d = \mu_n C_{ox} \frac{W}{L}\left[\frac{V_{DS}^2}{2} - V_{th}V_{DS}\right] \quad (4)$$

As the voltage level of virtual ground drops, V_{DS} over the ST drops, too; this makes the drain to source current of the ST I_d drops quadraticly. The dropping I_d decreases the voltage fluctuation on the ground and power net, which will be shown in the simulation results section. When the V_{DS} over the ST is low enough, it can be switched to the next stage.

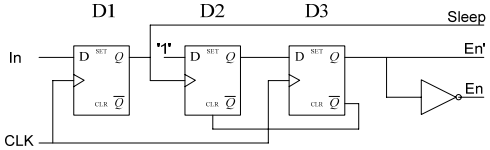


Figure 7. Control signal generating circuits

In stage II–the completely turned-on stage, the small transistor is turned off. The transmission gate is turned on to allow the sleep signal to turn on the ST.

For those chips without PMU, the proposed scheme can also be implemented by using a wake-up signal generating circuit, as shown in Figure 7. In Figure 7, D1~D3 are D type flip-flops with reset terminals. When the circuit is turned on from sleep mode, the input signal 'In' is switched from '0' to '1', and then it propagates through the D type flip-flop D1, and output as 'Sleep' signal. 'Sleep' signal is also used as the clock input of D2, thus the data input of D2 is propagated through D2 and D3 and appear at last as 'En", at the same time, D2 is reset by the inverse data output of D3, therefore, 'En" is reset one clock cycle later. An inverter is used to obtain 'En'.

If the relaxation stage lasts for a period of time which is long enough, the virtual ground will stay near 0. This can be illustrated by the equivalent circuit in Figure 6(a).

In Figure 6(b), the resistance of the circuit CT_1 is assumed as r_1, and the voltage V_G at node must satisfy Eq. (5):

$$\frac{V_{DD} - V_G}{r_1} = \mu_n C_{ox} \frac{W}{L}\left[\frac{V_G^2}{2} - V_{th}V_G\right] \quad (5)$$

From Eq.(5), $V_G = 0$ is not a solution, thus V_G keeps at a value above zero and is decided by the ST size and its threshold voltage.

The advantage of the proposed scheme is that: 1) the control transistor M_C and the transmission gate TG are not on the current path, thus they can use the smallest size; 2) the discharge current and the final voltage level of virtual ground during relaxation stage are determined only by the ST itself, which simplify the design procedure. The penalty is that the proposed scheme requires some control power to turn on M_C and TG.

3. Intermediate state circuit schemes

To further reduce the ground bounce and wakeup time, both the virtual power and ground should be set at a medium voltage value between V_{DD} and ground, that is, an intermediate state in the sleep mode. In this section, based on our proposed power gating scheme, we propose two improved circuit schemes which allow the circuit to stay at intermediate states.

3.1. Intermediate scheme I

In some applications, the output states of the circuits need to be maintained during the sleep mode, thus the ST should not be completely turned off. We introduce *intermediate scheme I* to solve this problem. The analysis in section 2 implies that the relaxation stage can be used as an intermediate state, as shown in Figure 6(a). In this state, the virtual ground is near 0. Thus the output of the circuit CT_1 can be maintained, at the cost of a larger leakage power consumption. This idea is similar as the one proposed by Kim [7], which used a PMOS to set the intermediate state.

The leakage equivalent circuit in the intermediate state is shown in Figure 6(b). Because of a relatively large leakage current, scheme I is not energy efficient; however, it has a short wakeup time, and can be used in the applications that frequently switches between active and intermediate states.

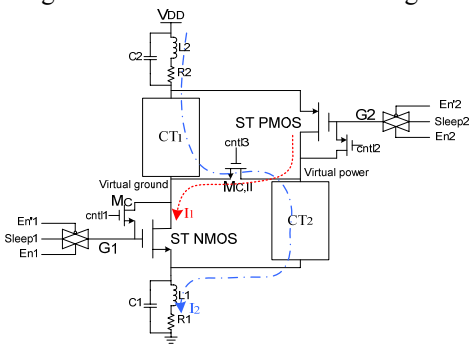
3.2. Intermediate scheme II

In some other applications, both the leakage and wakeup time are critical, so that we proposed *intermediate scheme II* to make a better tradeoff between leakage and wakeup time. In scheme II, the idea of charge recycling, which was proposed by Pakbaznia *et al.*[4], is extended and implemented. This scheme has to use NMOS and PMOS ST at the same time, as shown in Figure 8(a). The transmission gate method in [4] is replaced by a single NMOS transistor $M_{C,II}$.

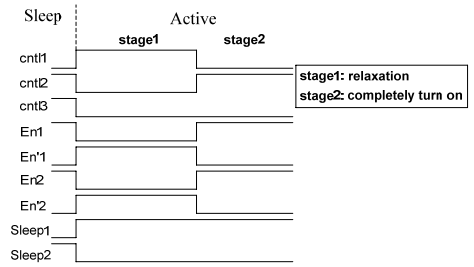
In the intermediate state, $M_{C,II}$ is turned on, and the virtual power and the virtual ground lines are set at about $V_{DD}/2$ by the transistor $M_{C,II}$, which is controlled by a control signal: 'cntl3'. To keep the virtual power and the virtual ground at the same level (about $V_{DD}/2$), the threshold voltage of the NMOS transistor $M_{C,II}$-- $V_{th,NMOS}$ should satisfy the inequality:

$$V_{th,NMOS} \leq V_{DD} - V_f \quad (6)$$

where V_f is the voltage level of virtual ground and virtual power. Generally, $V_f=V_{DD}/2$, thus the inequality can be rewrote as $V_{th,NMOS}<V_{DD}/2$, which can be guaranteed in most applications. When the circuits are turned to intermediate mode, the $M_{C,II}$ is turned on, this procedure can recycle some charge stored by CT_2 [4]. However, the single transistor $M_{C,II}$ will take a longer time than a transmission gate to make the virtual power and the virtual ground at almost the same level. Therefore, different from scheme I, scheme II is more suitable in the applications which have a long sleep time and require a quick wake-up. The timing of the control signals for scheme II is shown in Figure 8(b).



(a) Intermediate scheme II



(b) Timing of the control signal

Figure 8. Scheme II and control signals timing

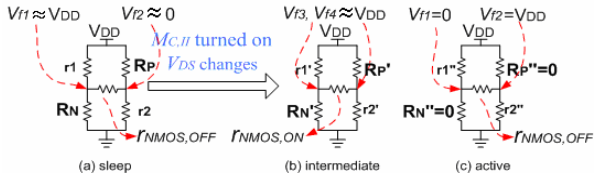


Figure 9. Equivalent circuit of intermediate scheme II for leakage estimation

3.3. Intermediate scheme leakage analysis

When using the intermediate scheme I, the intermediate state leakage current can be derived according to Eq. (5):

$$I_{leakage}=\frac{V_{DD}-V_G}{r_1}=\mu_n C_{ox}\frac{W}{L}\left[\frac{V_G^2}{2}-V_{th}V_G\right] \quad (7)$$

When using the intermediate scheme II, the leakage current is calculated as follows:

I. In the sleep state, $M_{C,II}$ and ST are all turned off. The equivalent circuit is shown in Figure 9(a). As mentioned in section 2, the virtual ground is charged to near V_{DD}, while virtual power is discharged to near ground. $M_{C,II}$ is on a major leakage path in this state. E. Pakbaznia *et al*.[4] gave a detailed analysis about this leakage, they deduced an formula about the effect of the transmission gate(replaced by $M_{C,II}$ in our proposed scheme) on the leakage increase.

II. In the intermediate state, $M_{C,II}$ is turned on while ST are turned off, whose equivalent circuit is in Figure 9(b). The leakage current can also be calculated by using Eq. (9), however, the V_{DS} of the ST changes, which has some effects on the circuit resistance. To illustrate this, first we make some assumptions: the cut-off drain-to-source resistances of the PMOS and NMOS ST are R_N and R_P; the resistance for the circuit CT_1 and CT_2 are r_1 *and* r_2 respectively. We further assume that $R_N=R_P=R_{ST}$, $r_1=r_2=r$; the turn-on drain-to-source resistance for the NMOS is $r_{NMOS,ON}$, while its turn-off resistance is $r_{NMOS,OFF}$. They satisfy $R_{ST}>r$, $r>>r_{NMOS,ON}\approx 0$.

For a turn-off ST, its drain-to-source resistance for leakage current is $R=1/(Gm_{ST})$; while $Gm_{ST}=d(I_{subthreshold})/dV_{DS}$ is the transconductance of the turned-off ST.

$$Gm_{ST}=\frac{d(I_{subthreshold})}{dV_{DS}}=\frac{I_0}{nV_{th}}e^{\frac{(V_{gs}-V_t+\eta V_{DS})}{nV_{th}}}\left[\eta-(\eta-n)e^{\frac{-V_{DS}}{V_{th}}}\right] \quad (8)$$

The above equation show that, if V_{DS} of a transistor decreases, its drain-to-source resistance decreases, too. Since in the intermediate state, the V_{DS} is different from the one in the sleep mode, therefore, the R_{ST}, r are different, either; hence we should recalculate the resistance for more accurate leakage approximation.

III. In the active state, the transistor $M_{C,II}$ is turned off while ST are turned on. The equivalent circuit is in Figure 9(c). The drain-to-source current of $M_{C,II}$ is V_{DD}. Thus the leakage current of $M_{C,II}$ can be calculated using Eq.(9).

$$I_{subthreshold}=I_0 e^{\frac{(V_{gs}-V_t+\eta V_{DS})}{nV_{th}}}\left(1-e^{\frac{-V_{DS}}{V_{th}}}\right) \quad (9)$$

From Eq.(9), it can be inferred that by using high V_{th} in $M_{C,II}$, the leakage current can be suppressed,

however, in order to guarantee the inequality (5), the V_{th} of $M_{C,II}$ can not be too high.

HSPICE simulation shows that, in 180nm technology, if $M_{C,II}$ is turned on to set at intermediate state, the $R'_{N,P} \approx 0.85R_{N,P}$, $r'_{1,2} \approx 1.25r_{1,2}$. In our benchmark, when ST is turned off, the virtual ground is charged to about 1.7V (1.8V supply), and the virtual power is discharge to about 0.1V, thus we obtained that $R_{ST} \approx 17r$. Finally we can estimate that, the leakage power in intermediate state (using scheme II) is about 4 times as the one in the sleep mode.

4. Simulation results

We used HSPICE to simulate the ground bounce effect and energy consumption during mode transition, using the ISCAS85 benchmark for TSMC 180nm CMOS technology. The supply voltage is set at 1.8V, and the relaxation time is fixed at 5ns. And the wakeup time is defined as the time between when the sleep signal is switched and the time when the fluctuation of the virtual ground and virtual power is less than 5% of the supply [2].

4.1. Linear resistance ST scheme simulation

In the simulation, we compare the wakeup time with (W) and without (WO) our proposed scheme. The simulation result is shown in Table 1.

The simulation result shows that the wakeup time can be reduced by 62.35% on average if our proposed scheme implemented.

Figure 10 shows the C432's virtual ground voltage transition during the wakeup procedure, which occurs at 10ns. When using our proposed scheme, as the dash line shown in Figure 10, it is clear that there are stages: 10n~15ns is the relaxation stage, in which the virtual ground voltage drops in a relatively smooth manner. Beyond 15ns is the completely turn-on stage, since the virtual ground has dropped low enough, the fully turn-on of the ST causes less fluctuation compared to the one without our proposed scheme.

The peak current and voltage glitch reduction are also simulated, which is shown in Table 2.

From table 2, the reduction of the peak voltage reduction is about 67.00% and the peak current reduction is about 79.00%. The ST in linear-resistance region greatly limits the transient current during the relaxation period. Moreover, this current is uniform, as shown in Figure 11(C432).

4.2. Intermediate schemes simulation

For the proposed intermediate states, we simulate the wakeup time from intermediate state to active state. And we also compare the leakage power in the intermediate state with the one in the sleep state.

Table 3 and 4 show the simulation results when implementing intermediate scheme I and II separately.

The results in Table 3 and 4 show that, when using the intermediate states, the wakeup time can be reduced further more. Intermediate scheme I can reduce 95.7% and intermediate scheme II can reduce 81.1% on average. These two schemes will consume more leakage, when using intermediate scheme I, the leakage is about 7 times of the sleep state, when using intermediate scheme II, the leakage is about 4 times of the sleep state.

From Table 3 and 4, the two intermediate schemes provide a tradeoff between leakage and wakeup time. Therefore, they provide more flexibility.

5. Conclusions

In this paper, we introduce a new power gating scheme that can reduce ground bounce. Two intermediate schemes are also introduced to reduce the wakeup time. The HSPICE simulation of the ISCAS85 benchmark shows that the circuit reliability can be improved by using our proposed scheme: the maximum voltage glitches reduction on virtual power and virtual ground can be reduced up to about 67.00% on average, and the wakeup time saving is about 62.3% on average. Furthermore, by using the proposed intermediate schemes I and II, the wakeup time can be reduced greatly at the expense of extra energy consumption: In particular, scheme I can achieve 95.7% wakeup time reduction while consumes 7 times leakage; and scheme II can achieve 81.1% wakeup time reduction while consumes 4 times leakage.

Table 1. Wakeup time simulation results

Circuit	Wakeup time (ns)		Wakeup time Reduction
	WO	W	
C432	26.50	5.60	78.80%
C499	23.00	9.70	57.80%
C880	31.50	11.00	65.00%
C1355	25.90	11.30	56.30%
C1908	27.50	9.90	64.00%
C2670	23.60	12.10	48.70%
C3540	29.00	10.80	62.70%
C5315	25.50	11.00	56.80%
C6288	37.40	14.30	61.70%
C7552	33.50	11.00	67.10%
Avg	28.34	10.67	62.30%

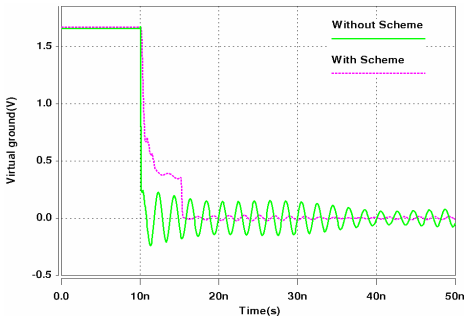


Figure 10. Virtual ground voltage during mode transition

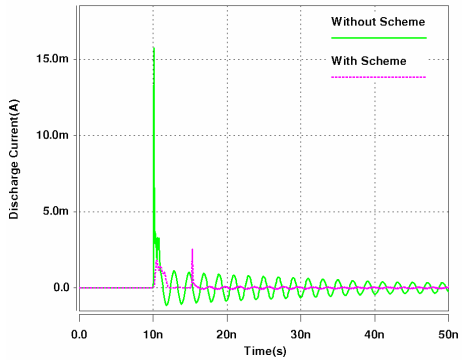


Figure 11. Discharge current during mode transition

Table 2. Peak current and voltage glitch reduction (WO/W)

Circuit	Power net peak voltage(V)	Ground net peak voltage(V)	Peak discharge current(mA)
C432	0.20/0.05	0.24/0.07	15.70/2.50
C499	0.48/0.16	0.36/0.12	23.50/5.50
C880	0.35/0.12	0.37/0.12	24.10/3.50
C1355	0.34/0.12	0.45/0.14	26.50/4.70
C1908	0.33/0.12	0.34/0.10	27.00/3.70
C2670	0.51/0.18	0.58/0.25	33.00/9.00
C3540	0.45/0.13	0.41/0.10	32.40/4.80
C5315	0.57/0.18	0.58/0.20	36.70/8.80
C6288	0.33/0.19	0.50/0.19	38.20/11.00
C7552	0.60/0.18	0.60/0.21	40.50/9.00
Avg	0.42/0.14	0.44/0.15	29.76/6.25

6. Acknowledgement

This work was supported by grant from National Natural Science Foundation of China No. 60506010 and the Project funded by Basic Research Foundation of School of Information Science and Technology of Tsinghua No SIST2017.

Table 3. Wakeup-time saving and leakage power (Scheme I)

Circuit	Wakeup time(ns)	Intermediate leakage power (nW)	Sleep leakage power (nW)
C432	0.70	8.14	2.66
C880	0.80	23.70	3.44
C1355	1.00	24.80	3.77
C1908	1.00	26.90	4.10
C3540	1.00	37.00	4.75
Avg	1.20	24.11	3.74

Table 4. Wakeup-time saving and leakage power (Scheme II)

Circuit	Wakeup time(ns)	Intermediate leakage power (nW)	Sleep leakage power (nW)
C432	1.10	6.33	3.37
C880	2.30	16.80	4.28
C1355	8.60	17.54	4.68
C1908	7.20	19.26	5.05
C3540	8.90	26.30	5.81
Avg	5.62	17.25	4.64

7. References

[1] S. Mutoh, et al, "A 1-V Power Supply High-Speed Digital Circuit Technology with Multi-threshold Voltage CMOS", *JSSC*, Vol. SC-30, 1995, pp.847-854.

[2] S. Kim, S.V. Kosonocky, Stephen, and D.R. Knebel, "Understanding and Minimizing Ground Bounce during Mode Transition of Power Gating Structures", *Proc. ISLPED*, 2003, pp. 22-25.

[3] H.S. Deogun, D. Sylvester, and K. Nowka, "Fine Grained Multi-threshold CMOS for Enhanced Leakage Reduction", *Proc. ISCAS*, 2006, pp. 3850-3853.

[4] E. Pakbaznia, F. Fallah, and M. Pedram, "Charge Recycling in MTCMOS Circuits: Concept and Analysis", *Proc. DAC*, 2006, pp. 97-102.

[5] P. Heydari, and M. Pedram, "Ground Bounce in Digital VLSI Circuits", *IEEE Trans. on VLSI systems*, Apr.2003, pp. 180-193.

[6] A. Abdollahi, F. Fallah, and M. Pedram, "An Effective Power Mode Transition Technique in MTCMOS", *Proc. DAC*, 2005, pp. 37-42.

[7] S. Kim, S.V. Kosonocky, D. R. Knebel, and K. Stawiasz, "Experimental Measurement of a Novel Power Gating Structure with Intermediate Power Saving Mode", *Proc. ISLPED*, 2004, pp. 20-25.

[8] S. Narendra, A. Chandrakasan, *Leakage in nanometer CMOS technologies*, Springer, 2005.

[9] Y. Chang, S. K. Gupta, and M. A. Breuer. "Analysis of ground Bounce in Deep Sub-micron Circuits", *Proc. VLSI Test Symposium*, 1997, pp. 110-116.

[10] S. Henzler, et al. "Sleep Transistor Circuits for Fine-Grained Power Switch-off with Short Power-down Times", *International Solid State Circuits Conference*, 2005, pp. 302-303.

[11] C. Long, L. He. "Distributed Sleep Transistor Network for Power Reduction", *Proc. DAC*, 2003, pp.181-186.